# AMENDMENT TRANSMITTAL LETTER

Docket No. M4065.0223/P223

| Application No. | Filing Date | Examiner | Group Art Unit |
|---|---|---|---|
| 09/517,314 | March 2, 2000 | D. Kang | 2811 |

Applicant(s): Chih-chen Cho



Invention: BACKEND METALLIZATION METHOD AND DEVICE OBTAINED THEREFROM

**TO THE COMMISSIONER FOR PATENTS**

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

| CLAIMS AS AMENDED | | | | | |
|---|---|---|---|---|---|
| | Claims Remaining After Amendment | Highest Number Previously Paid | Number Extra Claims Present | Rate | |
| **Total Claims** | 31 | - 38 = | | x | 0.00 |
| **Independent Claims** | 4 | - 5 = | | x | 0.00 |
| **Multiple Dependent Claims (check if applicable)** | ☐ | | | | |
| **Other fee (please specify):** | | | | | |
| **TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:** | | | | | 0.00 |

☒ Large Entity ☐ Small Entity

☒ No additional fee is required for this amendment.

☐ Please charge Deposit Account No. 04-1073 in the amount of $ _____. A duplicate copy of this sheet is enclosed.

☐ A check in the amount of $ _____ to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 04-1073 as described below. A duplicate copy of this sheet is enclosed.

☒ Credit any overpayment.

☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Dated: May 14, 2001

Thomas J. D'Amico
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#10/ Amdt A

PATENT
Docket No.: M4065.0223/P223

5/22/01
VS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE


In re Application of:
Chih-chen CHO

Serial No.: 09/517,314

Group Art Unit: 2811

Filed: March 2, 2000

Examiner: D. Kang

For: BACKEND METALLIZATION METHOD AND DEVICE OBTAINED THEREFROM



Commissioner for Patents
Washington, D.C. 20231

## AMENDMENT

Dear Sir:

Responsive to the Office action dated February 14, 2001, please amend the above-identified application as follows:

Cancel claims 2 and 19 and non-elected claims 33-38 without prejudice or disclaimer to the subject matter recited therein, amend the paragraph beginning on page 9, line 12 of the specification and claims 1, 9, 17, 18 and 26, and add new claim 39 as follows:

Page 9, line 12 – page 10, line 2:

Referring now to FIG. 8, a device constructed in accordance with the invention can be used in a memory circuit, such as a DRAM device 512, or other electronic integrated circuit, within a processor-based system 500. The processor-based system 500 may be a computer system, a process control system or any other system employing a processor and associated memory. The system 500 includes a central processing unit (CPU) 502, which may be a microprocessor. The CPU 502 communicates with the DRAM device 512, which has an array of cells 513 that include the semiconductor device 200 (or the semiconductor device 300), over a bus 516. The CPU 502 further communicates with one or more I/O devices 508, 510 over the bus 516. Although illustrated as a single bus, the bus 516 may be a series of buses and bridges commonly used in a processor-based system. Further components of the system 500 may include a read only memory (ROM) device 514 and peripheral devices such as a floppy disk drive 504, and CD-ROM drive 506. The floppy disk drive 504 and CD-ROM drive 506 communicate with the CPU 502 over the bus 516.

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1. (Amended) A semiconductor structure comprising:

an insulator layer;

a conductive plug positioned within said insulator layer;

an etch-stop layer located on said insulator layer and surrounding said plug;

a non-conductive layer having an etched via at least partially over said conductive plug; and

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a conductive connector formed in said via in electrical contact with said plug and including a first conductive layer deposited in and in contact with said etched via and a second conductive layer deposited over said first conductive layer, said first conductive layer including a portion in contact with said conductive plug.

9. (Amended) The semiconductor structure of claim 1, wherein said first conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

17. (Amended) The semiconductor memory device of claim 11, further comprising a plurality of said memory cells.

18. (Amended) A semiconductor device comprising:

a conductive element;

an etch-resistant layer surrounding an upper portion of said conductive element;

a non-conductive layer over said etch resistant layer and having a via over said conductive element, said via extending down to a level of said conductive element and etch resistant layer;

a conductive material located in said via, wherein said conductive material

contacts said conductive element; and

a doped region connected to said conductive element.

26. (Amended) The processor-based system of claim 25, wherein said conductive connector further comprises a second conductive layer deposited over said first conductive layer.

39. (New) The semiconductor memory device of claim 17, wherein said plurality of said memory cells are in an array.